Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The final Office Action dated August 10, 2005, indicated that claims 1-12 and 17-19 are rejected under 35 U.S.C. § 102(e) over Yang (U.S. Patent No. 6,113,462) and claims 14-16 are rejected under 35 U.S.C. § 103(a) over Yang in view of Hu *et al.* (U.S. Patent No. 6,227,947).

Applicant maintains the traversal of the prior art rejections (Section 102(e) and Section 103(a)) because the Examiner fails to present a reference or combination of references that corresponds to the claimed invention. No teachings have been identified, and no extrinsic evidence has been provided to indicate, that the '462 reference corresponds to or inherently teaches the claimed invention. For example, the Examiner fails to identify where the '462 reference teaches positioning the wafer carrier misaligned with respect to the pad as a function of the wafer being polished in the center-offset manner. The citations to the '462 reference fail to teach or suggest any intentional positioning of the wafer as such, and the Examiner does not even assert at pages 2-3 of the Office Action that the '462 reference corresponds to these limitations which are found in each of the independent claims.

The Examiner also fails to identify any teachings in the '462 reference that are directed to removing the wafer from the carrier and manually inspecting the wafer (*e.g.*, claim 3). In contrast, the '462 reference is directed to automatically correcting the non-uniform effects of pad wearing using a feedback loop. *See* column 3, lines 56-61 and column 4, lines 60-63.

The Examiner has also not asserted or identified that the '462 reference teaches structure corresponding to the claimed means for determining whether the wafer is polishing in a center-offset manner (*e.g.*, claims 11 and 17). Applicant notes that at page 7, lines 11-13, of the Specification, one method for detecting whether the wafer is being polished in a center-offset manner is identified as removing the wafer from the carrier and measuring the thickness across the wafer using a device such as a pair of calipers. Without an assertion or presentation of correspondence to each of the claimed limitations, the Section 102(e) and Section 103(a) rejections cannot be maintained.